Amendment To The Claims

Claims 1-8 Canceled

9. (Original) A reference voltage buffering circuit provided in a source driver circuit for driving a liquid crystal element of a liquid crystal module, wherein:

the reference voltage buffering circuit comprises two buffering circuits arranged in parallel to each other between an input-side node for receiving an externally produced reference voltage as an input voltage and an output-side node for sending out an output voltage; and

each of the buffering circuits includes:

an operator for receiving the input voltage at one terminal and an output voltage of the operator itself at the other terminal, and operating so that the output voltage is equal to the input voltage;

a capacitor including a first electrode and a second electrode for storing a charge corresponding to a voltage difference between the input voltage and the output voltage;

a first node connected to the first electrode of the capacitor;

a second node connected to the second electrode of the capacitor;

a third node for receiving an output signal from the operator;

a first switching element provided between the second node and the third node;

a second switching element provided between the first node and the input side of the operator;

a third switching element provided between the first node and the output-side node; and

a fourth switching element provided between the third node and the output-side node.

10. (Original) The reference voltage buffering circuit of claim 9, further comprising a closed circuit added to the second node, the closed circuit including therein a fifth switching element for compensating for an electric change in the second node due to switching of the first switching element.

11. (Original) A method for controlling a reference voltage buffering circuit, including two buffering circuits arranged in parallel to each other, each of the buffering circuits including: an operator provided between an input-side node and an output-side node for operating so that an output voltage is equal to an input voltage; a capacitor including a first electrode and a second electrode; a first node connected to the first electrode of the capacitor; a second node connected to the second electrode of the capacitor; a third node for receiving an output signal from the operator; a first switching element provided between the second node and the third node; a second switching element provided between the first node and the input side of the operator; a third switching element provided between the first node and the output-side node; and a fourth switching element provided between the third node and the output-side node, wherein:

in each of the buffering circuits, in an output mode in which a reference voltage is output from the buffering circuit, the third and fourth switching elements are placed in a conductive state while the first and second switching elements are placed in a non-conductive state; and

in a charge storing mode in which the capacitor of the buffering circuit stores a charge, the third and fourth switching elements are placed in a non-conductive state while the first and second switching elements are placed in a conductive state.

12. (Original) The method for controlling a reference voltage buffering circuit of claim 11, wherein:

the reference voltage buffering circuit further includes a closed circuit added to the second node, the closed circuit including therein a fifth switching element for canceling out an electric change in the second node due to switching of the first switching element; and

when the first switching element is switched between a conductive state and a non-conductive state from one to another, the fifth switching element is switched reversely in an interlocking manner.

13. (Original) The method for controlling a reference voltage buffering circuit of claim 11 or 12, wherein:

when switching from a state where one of the two buffering circuits is in the output mode while the other buffering circuit is in the charge storing mode to another state where the one buffering circuit is in the charge storing mode while the other buffering circuit is in the output mode,

the third and fourth switching elements of the other buffering circuit are switched to a conductive state after the third and fourth switching elements of the one buffering circuit are switched to a non-conductive state.

14. (Original) The method for controlling a reference voltage buffering circuit of claim 13, wherein:

when the third and fourth switching elements of the one buffering circuit are switched to a non-conductive state, the third switching element is switched to a non-conductive state after the fourth switching element is switched to a non-conductive state; and

when the third and fourth switching elements of the other buffering circuit are switched to a conductive state, the fourth switching element is switched to a conductive state after the third switching element is switched to a conductive state.

Claims 15-17 Canceled

18. (New) A liquid crystal driving circuit for driving a liquid crystal element in which a plurality of source driver circuit devices having an input-side pad unit including a plurality of input-side pads and an output-side pad unit including a plurality of output-side pads are arranged on a liquid crystal panel, the liquid crystal driving circuit comprising:

a reference voltage production circuit capable of producing a plurality of reference voltages to drive the plurality of source driver circuit devices; and

a reference voltage wire unit capable of receiving the plurality of reference voltages and providing the plurality of reference voltages to the plurality of source driver circuit devices,

the reference voltage wire unit including;

a plurality of in-chip reference voltage wire units, each in-chip reference voltage wire unit being configured in each source driver circuit device of the plurality of source driver circuit devices, and including a plurality of in-chip reference voltage wires, each in-chip reference voltage wire connecting each input-side pad in the input-side pad unit to each output-side pad in the output-side pad unit; and

a plurality of inter-chip reference voltage wire units, each inter-chip reference voltage wire unit being configured between any two adjacent source driver circuit devices of the plurality of source driver circuit devices and including a plurality of inter-chip reference voltage wires, each inter-chip reference voltage wire connecting each output-side pad in the output-side pad unit of one source driver circuit device of the two adjacent source driver circuit devices to each input-side pad in the input-side pad unit of the other source driver circuit device of the two adjacent source driver circuit devices.

19. (New) The liquid crystal driving circuit of claim 18, further comprising a reference voltage providing wire unit including a plurality of reference voltage providing wires, each reference voltage providing wire extending from the reference voltage production circuit and connecting to each input-side pad in the input-side pad unit of one of the plurality of source driver circuit devices,

wherein the reference voltage providing wire unit, the plurality of in-chip reference voltage wire units and the plurality of inter-chip reference voltage wire units form a single continuous wiring structure via each input-side pad unit and each output-side pad unit of the plurality of source driver circuit devices.

20. (New) The liquid crystal driving circuit of claim 18, each source driver circuit device of the plurality of source driver circuit devices including:

a plurality of branch reference voltage wires, each branch reference voltage wire branching off from each in-chip reference voltage wire of the in-chip reference voltage wire unit;

a plurality of buffers, each buffer receiving a reference voltage supplied from each branch reference voltage wire of the plurality of branch reference voltage wires, and thereafter outputting an output voltage; and

a selection circuit selecting any one of the reference voltages supplied from the plurality of buffers and outputting the selected reference voltage to each of a plurality of wires extending to the liquid crystal element as a voltage for driving the liquid crystal element.

21. (New) The liquid crystal driving circuit of claim 20, each source driver circuit device of the plurality of source driver circuit devices further comprising a plurality of subdivided voltage production circuits, each subdivided voltage production circuit receiving output from each buffer of the plurality of buffers so as to produce subdivided voltages, and thereafter outputting the subdivided voltages to the selection circuit,

wherein the selection circuit selects one of the subdivided voltages as the voltage for driving the liquid crystal element.

22. (New) The liquid crystal driving circuit of claim 20, wherein the plurality of buffers include a first buffer receiving a positive-side reference voltage having a higher voltage than a predetermined voltage and a second buffer receiving a negative-side reference voltage having a lower voltage than the predetermined voltage,

each source driver circuit device of the plurality of source driver circuit devices further includes:

a positive-side voltage production circuit receiving an output voltage of the first buffer so as to produce positive subdivided voltages as the subdivided voltages, and thereafter outputting the positive subdivided voltages to the selection circuit; and

a negative-side voltage production circuit receiving an output voltage of the second buffer so as to produce negative subdivided voltages as the subdivided voltages, and thereafter outputting the negative subdivided voltages to the selection circuit, and

the selection circuit of each source driver circuit device selects a positive output and a negative output from the positive subdivided voltages and the negative subdivided voltages such that any two adjacent wires of the plurality of wires extending to the liquid crystal element alternately receive the positive output and the negative output at regular time intervals.

23. (New) A semiconductor integrated circuit device provided in a liquid crystal module having a liquid crystal element, the semiconductor integrated circuit comprising:

an input-side pad unit including a plurality of input-side pads, each input-side pad receiving a plurality of reference voltages;

an output-side pad unit including a plurality of output-side pads, each output-side pad outputting the plurality of reference voltages;

an in-chip reference voltage wire unit including a plurality of in-chip reference voltage wires directly connecting each input-side pad of the input-side pad unit to each output-side pad of the output-side pad unit to transmit the plurality of reference voltages;

a plurality of branch reference voltage wires, each branch reference voltage wire branching off from each in-chip reference voltage wire of the in-chip reference voltage wire unit;

a plurality of buffers, each buffer receiving a reference voltage supplied from each branch reference voltage wire of the plurality of branch reference voltage wires, and thereafter supplying an output voltage; and

a selection circuit selecting a voltage for driving the liquid crystal element from the output voltages of the plurality of buffers.

24. (New) The semiconductor integrated circuit device of claim 23, further comprising a subdivided voltage production circuit receiving each output voltage of the plurality of buffers so as to produce subdivided voltages, and thereafter outputting the subdivided voltages,

wherein the selection circuit selects one of the subdivided voltages as the voltage for driving the liquid crystal element.

25. (New) The semiconductor integrated circuit device of claim 23, further comprising a positive-side voltage production circuit receiving an output voltage of a first buffer of the plurality of buffers so as to produce positive subdivided voltages as the subdivided voltage, and thereafter outputting the positive subdivided voltages to the selection circuit; and

a negative-side voltage production circuit receiving an output voltage of a second buffer of the plurality of buffers so as to produce negative subdivided voltages as the subdivided voltage, and thereafter outputting the negative subdivided voltages to the selection circuit,

wherein the first buffer receives a positive-side reference voltage having a higher voltage than a predetermined voltage, and the second buffer receives a negative-side reference voltage having a lower voltage than the predetermined voltage,

the selection circuit selects a positive output and a negative output from the positive subdivided voltages and the negative subdivided voltages such that any two adjacent wires of the plurality of wires extending to the liquid crystal element alternately receive the positive output and the negative output at regular time intervals.

26. (New) The semiconductor integrated circuit device of claim 23, wherein each input-side pad of the input-side pad unit is configured along one side of the semiconductor integrated circuit device, and

each output-side pad of the output-side pad unit is configured along another side of the semiconductor integrated circuit device.

27. (New) The semiconductor integrated circuit device of claim 23, wherein each buffer of the plurality of buffers has an offset canceling function capable of reducing a potential difference between an input voltage and an output voltage.

28. (New) The semiconductor integrated circuit device of claim 27, wherein each buffer of the plurality of buffers includes:

an operator capable of receiving an input voltage of the buffer at one terminal and an output voltage of the operator at the other terminal, so as to operate such that the output voltage is substantially equal to the input voltage;

a capacitor including a first electrode and a second electrode and capable of storing a charge corresponding to a voltage difference between the input voltage and the output voltage;

a first node connected to the first electrode of the capacitor;

a second node connected to the second electrode of the capacitor;

a third node for receiving the output voltage from the operator;

a first switching element provided between the second node and the third node;

a second switching element provided between the first node and a node on an input side of the operator;

a third switching element provided between the first node and a node on an output-side of the operator; and

a fourth switching element provided between the third node and the node on the output-side of the operator.

29. (New) The semiconductor integrated circuit device of claim 28, further comprising a closed circuit added to the second node, the closed circuit including a fifth switching element for compensating an electric change in the second node due to the switching of the first switching element.

30. (New) The semiconductor integrated circuit device of claim 27, wherein each buffer of the plurality of buffers includes;

an operator capable of receiving the input voltage of buffer at one terminal and an output voltage of the operator at the other terminal, so as to operate such that the output voltage is substantially equal to the input voltage;

a capacitor including a first electrode and a second electrode and storing a charge corresponding to a voltage difference between the input voltage and the output voltage;

an input-side node for introducing the input voltage to the operator;

a first node connected to the first electrode of the capacitor;

a second node connected to the second electrode of the capacitor;

a third node for receiving an output voltage from the operator;

a first switching element provided between the second node and the third node;

a second switching element provided between the first node and the input-side node of the operator; and

a third switching element provided between the first node and the third node.